



# Computer Engineering

## CE Program Seminar



### Rakesh Kumar

UCSB / CE Program Faculty Candidate from the University of California, San Diego

**Tuesday, January 17, 2006 ~ 9:00 am ~ Engineering Science Bldg (ESB), Room 2001**

#### *Heterogeneous Multi-core Computing*

We are on the cusp of a major technology shift. We are moving to an era where a single chip will likely be a massively parallel, computationally dense, and power-limited behemoth. In this talk, I will present Single-ISA Heterogeneous Multi-Core Architectures. These architectures recognize the diversity in workloads and adapt to them. A heterogeneous architecture consists of cores with different power/performance characteristics on the same die. Applications are then mapped to the "best-fit" cores for efficient execution.

An example heterogeneous multi-core architecture demonstrated up to six-fold improvement in energy efficiency for individual applications, and a three-fold improvement on average. The extent of power savings that was achieved is at least two times more than any other reported architectural technique, including frequency/voltage scaling and clock gating. A representative heterogeneous multi-core architecture using two core types also achieved a 63% performance improvement over an equivalent-area conventional chip multiprocessor. The throughput benefits were achieved without any loss of single-thread performance.

#### Speaker Bio

Rakesh Kumar is a PhD Candidate in the Department of Computer Science and Engineering at the University of California, San Diego. His research interests include multicore and multithreaded architectures, low-power architectures, and on-chip interconnects. Rakesh received a BS in computer science and engineering from the Indian Institute of Technology (IIT), Kharagpur. He is a recipient of the IBM PhD Fellowship and a CalRA Fellowship. He is a member of the ACM and was most recently a Program Chair of the Workshop on Design, Architecture, and Simulation of Chip Multiprocessors (dasCMP).



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