

Computer Engineering Program Seminar

“High-Performance RF and High-Speed Circuits in Scaled CMOS”

DR. C. PATRICK YUE
Carnegie Mellon University

DATE: Friday, October 14, 2005
TIME: 9:00 AM
LOCATION: Engineering Science Building (ESB), Room 2001

In this seminar, Prof. Yue will discuss the importance of device layout and bias conditions for maximizing RF performance and present a cell-based RF design methodology which mitigates the problems due to the immense complexity of high-frequency parasitic effects in circuit components. The concept of cell-based design exploits a unique property of RF circuits comprising a small set of re-usable sub-circuits and a large number of passive components, especially inductors. In contrast to conventional RF design flow, which uses pre-characterized individual devices, the sub-circuit-based approach alleviates the crucial, but often overlooked, problems due to the difference between the pre-characterized devices and the actual circuit layout. He will describe a physical model for on-chip spiral inductors which accounts for high-frequency phenomena such as skin and proximity effects. This model serves as a basis for an inductor layout optimization tool. He will then talk about the design of a patterned ground shield (PGS) to improve inductor performance. The PGS eliminates substrate loss and suppresses substrate noise coupling due to electric field penetration into the silicon substrate, which is critical for single-chip integration of RF and digital circuits.

Prof. Yue will also present some recently developed low-voltage RF receiver circuits. His group has designed a 1-V 3.3-mW ultra-wideband mixer in 0.13-um CMOS. To facilitate low-voltage operation, the mixer employs a folded Gilbert cell topology with PMOS devices for LO switches and utilizes on-chip broadband RF chokes for biasing. To push the integration level of RF transceivers, he will describe a 5-GHz transmit/receive switch with matching networks in a 0.18-um CMOS process. The T/R switch employs a novel LC-tuned substrate biasing technique to handle voltage swings up to 10-V_{pp} while matched to 50-ohm loads under a 1.8-V supply. This design achieves the highest linearity reported to date for CMOS RF switches.

As the clock speed increases, digital circuits are becoming analog-like, which inspires innovative application of analog techniques to solve digital system problems. Prof. Yue has worked on a 10-GHz global clock distribution with sub-pico-second skew and jitter, in 0.18-um CMOS process, using coupled standing-wave oscillators (SWOs). This work is the first demonstration of SWO on silicon. His group is currently developing a low-power continuous-time adaptive passive equalizer utilizing on-chip RLC components to compensate for the high-frequency attenuation in a lossy channel. The equalizer can compensate the loss of a 5-m CAT-5 cable at 20 Gb/s while consuming less than 10 mW.

C. Patrick Yue (S'93-M'98-SM05) received his B.S. degree from the University of Texas at Austin in 1992, and his M.S. and Ph.D. degrees in E.E. from Stanford University in 1994 and 1998, respectively. He is currently an Assistant Professor of Electrical and Computer Engineering at Carnegie Mellon University. His research focuses on high-frequency analog circuit design, RF device modeling, and design methodology to bridge the gap between these two areas. Prior to joining CMU, he has been a Consulting Assistant Professor at Stanford University and a founder of Atheros Communications in Silicon Valley. In 2002, he joined Aeluros, another fabless startup, focusing on signal integrity and device modeling issues.

Prof. Yue has published over 40 technical papers and one book chapter. He currently holds 11 U.S. patents. He is a co-recipient of the 2003 ISSCC Jack Kilby Best Student Paper Award. He currently serves on the Technical Program Committees of RFIC Symposium, Asian Solid-State Circuit Conference and the VLSI Circuit and Technology Committee for the IEEE Electron Devices Society. He is a Senior Member of the IEEE.

Departmental Host: Margaret Marek-Sadowska, Professor and Director Computer Engineering Program

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